MECOTrainings

Title: **Advanced Training in High Performance Embedded Systems**

Venue: Hotel Slovenska Plaza, Budva, Montenegro

Date: 09. 06-14. 06. 2019

Description: The training is intended for all those who want to acquire real-life knowledge from advanced embedded systems. The equivalent load of the 5 days training seminar is 3 ECTS credits. The main topics are: Recent challenges in Embedded computing, Cyber Physical and Internet of Things design, advanced FPGA design, Cutting-edge DSP processors, Code Optimization, Real-time operation systems, Real-time signal and image processing. Most lessons will be followed with practical exercises. The detailed agenda is given bellow, while more information could be obtained by Profs Naim Dahnoun and Dr. Sergey Vityazev (Naim.Dahnoun@bristol.ac.uk , vityazev.s.v@tor.rsreu.ru).

Price: The training fee is €350. The accommodation prices in Slovenska Plaza for FB are: in 3* hotel €36 in 1/ 2 room and €43 in 1/ 1 room; in 4**** hotel 39,00€ in 1/ 2 room and €45 in 1/ 1.

The Excursion costs around €30 per person and the conference dinner €40 (not compulsory) per person. You can arrange the accommodation and social life by yourself (the fee is only compulsory).

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Training Program:

DAY 1 (09 June 2019): Preparation day

Course Number:	Lab	Brief content	No of hours	Lecturer
1. Training Introduction and welcome: Organizational issues	No	The vision and mission of the trainings. Principles of the work etc..	1	Prof. dr Radovan Stojanovic
2. Recent challenges in Embedded computing, Cyber Physical Systems and Internet of Things design	No	Prof. Lech Jozwiak will summarize its 40 years experience in digital and analog design and points the main challenges in CPS and IoT	2	Prof. dr Lech Jozwiak
3. Who is going to win in the nearly future FPGA or GPU to be used in DNN?	NO	TBA	2	Prof. dr Betim Cico

DAY 2 (10 June 2019): Lectures:

Course Number:	Lab	Brief content	No of hours	Lecturer
1. Introduction to Graphics Processor Units GPUs	No	Introduction to graphic processors. NVIDIA Roadmap Practical Application	4	Prof. dr Naim Dahnoun
2. Introduction to advanced FPGA design	YES	The comparison between FPGA and DSP based signal processing. Design flow of FPGA based SP. Serial Parallel. Examples (Arithmetic units, Simple filters and Transforms as FIR, IIR, Haar, wavelets, image processing…)	2 lessons + 2 exercises	Prof. dr Radovan Stojanovic

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DAY 3, (11 June 2019), Lectures

Course Number:	Lab	Brief content	No of hours	Lecturer
1. Introduction to Digital Signal Processors DSPs	No	Introduction to DSP, Development tools Implementation	3	Prof. dr Naim Dahnoun
2. Optimization	No	Code optimization methods using the TI Keystone processors (see Note 2 below)	2	Prof. dr Naim Dahnoun
3. Real time operating system SYS/BIOS	No	Introduction to Real-time Operating systems SYS/BIOS functionality (see Note 2 below)	3	Prof. dr Naim Dahnoun

DAY 4: (12 June 2019): Laboratory

Course Number:	Lab	Brief content	No of hours	Lecturer
1. Introduction to Code Composer Studio (CCS) development environment	YES	Introduction to the CCS. Implementation of a dot product in C, Code benchmarking. Code downloading at separate cores and running on the TMS320C6678 EVM	3	Dr. Sergey Vityazev
2. Optimization	YES	Dot product implementation in assembly. Optimization in assembly and C. Software pipelining. Parallel execution on VLIW	2	Dr. Sergey Vityazev

		architecture		
3. Real-time operating system SYS/BIOS	YES	Basic thread types in SYS/BIOS: Hwis, Swis, tasks and clocks. Using clock functions, events and heaps.	3	Dr. Sergey Vityazev

DAY 5: Discussion and Certification Ceremony (13 June 2019):

Couse Number:	**Lab**	**Brief content**	**No of hours**	**Lecturer**
Discussion, feedbacks, proposals for further projects	NA	The participants of the training will discuss about their opinions, give feedbacks and suggestion as well as proposals for sustainable further cooperation	2	All
Certificates issuing	NA	To each participant that successfully complete the summer school will be issued certificate in load of 3ECTS	1	All
Excursion and social life	NA	Will be organizing special excursion	5	All

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Instructors:

Prof. Lech Jóźwiak, Eindhoven University of Technology, with Radovan Stojanovic one of the MECO's establishers, about Prof. Jóźwiak .

Prof Radovan Stojanovic, University of Montenegro, Together with Lech Jóźwiak establisher of projects www.embeddedcomputing.me and MECO. One of the pioneers of the FPGA and SoC design at Balkan. about Prof. Stojanovic in Wikipedia.

Prof. Naim Dahnoun, Bristol University: the textbooks by Prof. N. Dahnoun **,** Digital Signal Processing Implementation and Multicore DSP: From Algorithms to Real-time Implementation on the TMS320C66x SoC . About Prof. N. Dahnoun .

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Dr Sergey Vityazev , Senior Lecturer – Ryazan State Radio Engineering University, about Dr Vityazev. Teaching multi-core DSP implementation on EVM C6678 board.

Prof. Dr. Betim Çiço, Epoka University, Tirana, Pioneer and long lasting contributions in fields of Advance Computer Architecture, Digital Electronics, FPGA, Artificial Intelligence and Robotics, etc in Albania and Western Balkan. About Prof. B. Cico **.**

Notes:

Note 1: Real-time Operating System, TI-RTOS (SYS/BIOS): This lecture is divided into three main sections: (1) Real-time scheduler that is composed of the hardware and software interrupts; the task, the idle, clock and timer functions, synchronisation and events, (2) the Dynamic Memory Management and (3) laboratory experiments.

Note 2: Software Optimisation, Linear Assembly, Interfacing C and Assembly: This lecture discusses the different levels of optimisation for multicore and shows how code can be optimised for a DSP core. This lecture also shows how to use intrinsics and interface C language with intrinsics and assembly code. Multiple examples showing how to optimise code by hand and using the tools are provided.

Note 3: FPGA**:** A field-programmable gate array is an integrated circuit designed to be configured by a customer or a designer in the process of prototyping. The FPGA configuration is generally specified using a hardware description language (VHDL or Verilog). In some sense it is intermediate phase in designing/manufacturing an application-specific integrated circuit (ASIC). The preparation phases before configuration is text description entry or block diagram (schematic) entry.

Note 4: GPUs- Graphics Processing Units, ***DNNs***: Deep Neural Networks

Note 5: DSP processors: are specialized microprocessors or microcontrollers, with its architecture optimized for signal processing tasks.